CDF Run IIB Silicon Upgrade

Director's Review

Aug.12-16, 2002

Brenna Flaugher

Run IIB Silicon Project Co-leader

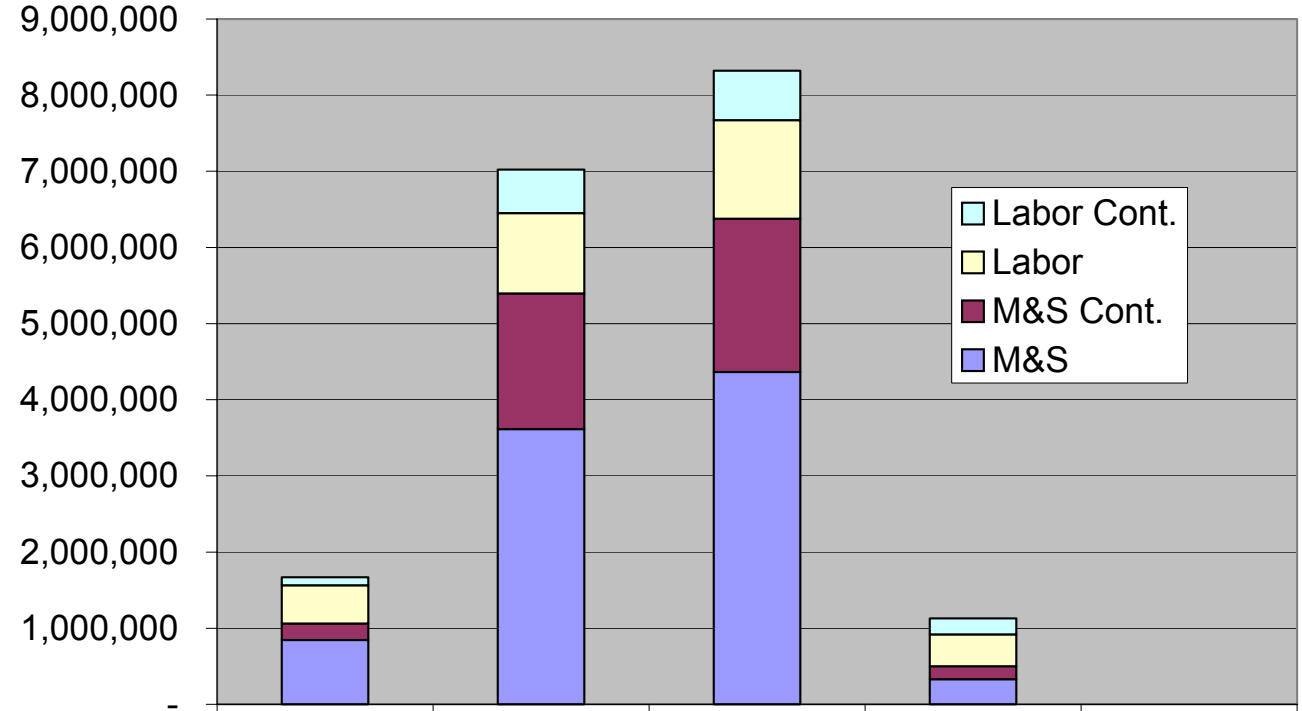
Fermilab

For the CDF Collaboration

Run IIb Silicon Technical Design

- Cost
  - Silicon Project Costs
  - Basis of estimate
- Schedule
  - reportable milestones and contingency
  - critical path
- Labor Profiles
- Risk Analysis
- Conclusions

Silicon Project Costs



Costs are in Then year $ and include overhead

	2002	2003	2004	2005	2006	
Labor Cont.	102,581	571,938	649,754	209,511	-	
Labor	502,549	1,055,130	1,292,582	419,191	-	Grand Total
M&S Cont.	218,914	1,778,400	2,012,040	169,843	-	
M&S	843,793	3,616,256	4,365,894	330,078	-	
Total (M$)	1.7	7.0	8.3	1.1	-	18.1

Silicon Project Costs

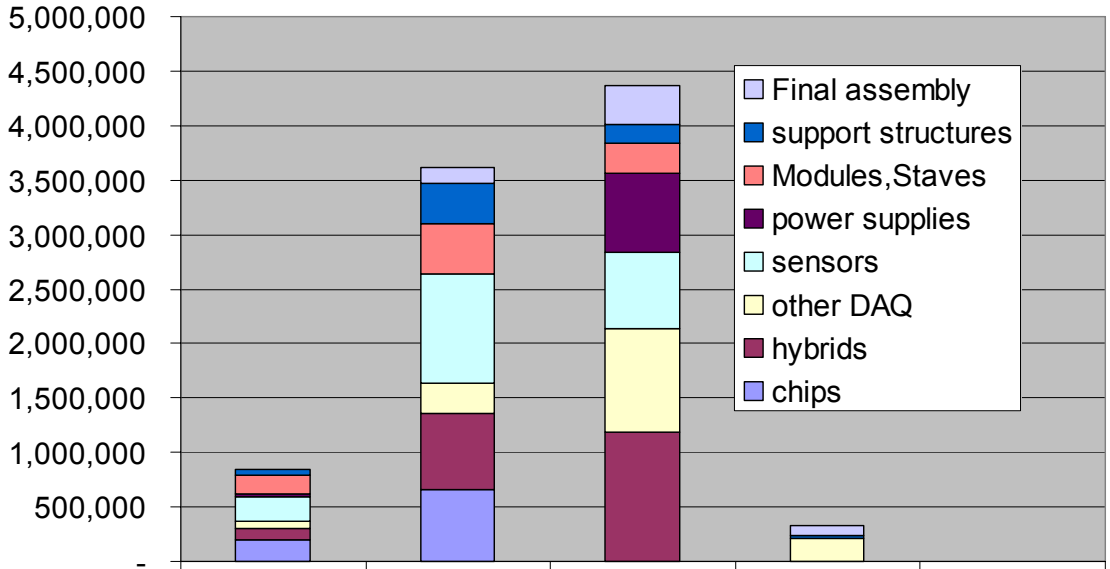
Costs in FY02 $ without overhead

	2002	2003	2004	2005	2006	Totals M$ FY02
M&S (FY02$)	723,665	3,037,630	3,579,670	263,091	-	7.6
M&S Cont. (FY02$)	187,748	1,493,844	1,649,705	135,374	-	3.5
Labor (FY02$)	389,573	801,107	957,936	302,002	-	2.5
Labor Cont. (FY02$)	79,520	434,243	481,535	150,940	-	1.1
Total (FY02$)	**1,380,506**	**5,766,824**	**6,668,846**	**851,408**	**-**	**14.7**

Costs in Then year $ including overhead

	2002	2003	2004	2005	2006	Totals M$
M&S	843,793	3,616,256	4,365,894	330,078	-	9.2
M&S Cont.	218,914	1,778,400	2,012,040	169,843	-	4.2
Labor	502,549	1,055,130	1,292,582	419,191	-	3.3
Labor Cont.	102,581	571,938	649,754	209,511	-	1.5
Total $	**1,667,837**	**7,021,723**	**8,320,270**	**1,128,623**	**-**	18.1

Silicon M&S Cost breakdown



	2002	2003	2004	2005	2006
Final assembly	2	151,194	353,343	95,716	-
support structures	57,445	360,400	176,847	18,819	-
Modules,Staves	164,066	466,292	276,809	-	-
power supplies	23,320	-	717,456	-	-
sensors	229,626	999,145	703,142	-	-
other DAQ	64,022	282,255	950,375	215,543	-
hybrids	108,419	701,684	1,187,923	-	-
chips	196,894	655,285	-	-	-

Costs are in Then year $ and include overhead

M&S Cost Breakdown

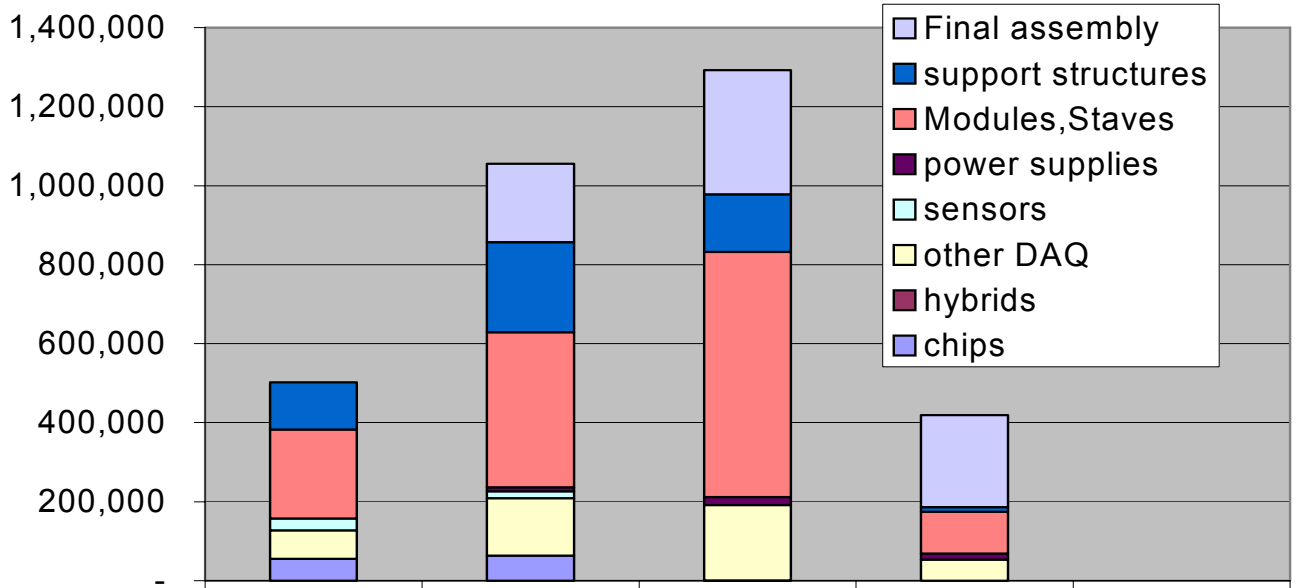
Costs in FY02 $ without overhead:

	2002	2003	2004	2005	2006	**Totals M$**
chips	168,863	550,435	-	-	-	**0.7**
hybrids	92,984	589,410	973,998	-	-	**1.7**
other DAQ	54,907	237,093	779,228	171,800	-	**1.2**
sensors	196,935	839,275	576,518	-	-	**1.6**
power supplies	20,000	-	588,254	-	-	**0.6**
Modules,Staves	140,708	391,682	226,960	-	-	**0.8**
support structures	49,267	302,733	145,000	15,000	-	**0.5**
Final assembly	2	127,002	289,712	76,291	-	**0.5**
Total $	**723,665**	**3,037,630**	**3,579,670**	**263,091**	**-**	**7.6**

Costs in Then Year $ including overhead:

	2002	2003	2004	2005	2006	**Totals M$**
chips	196,894	655,285	-	-	-	**0.9**
hybrids	108,419	701,684	1,187,923	-	-	**2.0**
other DAQ	64,022	282,255	950,375	215,543	-	**1.5**
sensors	229,626	999,145	703,142	-	-	**1.9**
power supplies	23,320	-	717,456	-	-	**0.7**
Modules,Staves	164,066	466,292	276,809	-	-	**0.9**
support structures	57,445	360,400	176,847	18,819	-	**0.6**
Final assembly	2	151,194	353,343	95,716	-	**0.6**
Total	**843,793**	**3,616,256**	**4,365,894**	**330,078**	**-**	**9.2**

Silicon Labor Cost Breakdown



	2002	2003	2004	2005	2006
Final assembly	-	197,976	314,422	232,739	-
support structures	119,806	228,398	145,597	11,999	-
Modules,Staves	225,074	392,295	620,925	105,304	-
power supplies	-	10,235	20,432	15,598	-
sensors	30,080	17,245	-	-	-
other DAQ	72,003	145,808	190,286	53,552	-
hybrids	-	-	-	-	-
chips	55,586	63,173	920	-	-

Costs are in Then year $ and include overhead

Silicon Labor Cost Breakdown

Costs in FY02 $ without overhead

	2002	2003	2004	2005	2006	**Totals M$**
chips	43,090	47,964	681	-	-	**0.1**
hybrids	-	-	-	-	-	**-**
other DAQ	55,816	110,704	141,022	38,581	-	**0.3**
sensors	23,318	13,093	-	-	-	**0.0**
power supplies	-	7,771	15,142	11,237	-	**0.0**
Modules,Staves	174,476	297,850	460,170	75,865	-	**1.0**
support structures	92,873	173,411	107,902	8,645	-	**0.4**
Final assembly	-	150,313	233,019	167,675	-	**0.6**
Total $	**389,573**	**801,107**	**957,936**	**302,002**	**-**	**2.5**

Costs in Then year $ including overhead

	2002	2003	2004	2005	2006	**Totals M$**
chips	55,586	63,173	920	-	-	**0.1**
hybrids	-	-	-	-	-	**-**
other DAQ	72,003	145,808	190,286	53,552	-	**0.5**
sensors	30,080	17,245	-	-	-	**0.0**
power supplies	-	10,235	20,432	15,598	-	**0.0**
Modules,Staves	225,074	392,295	620,925	105,304	-	**1.3**
support structures	119,806	228,398	145,597	11,999	-	**0.5**
Final assembly	-	197,976	314,422	232,739	-	**0.7**
Total	**502,549**	**1,055,130**	**1,292,582**	**419,191**	**-**	**3.3**

Cost: Basis of Estimate

- Costs (M&S and Labor) were derived in consultation with Run IIa project mechanical and electrical engineers
- BOE notebooks: quotations, drawings and the Run IIa schedule which were all used to estimate the costs.
- In general: 50% contingency on M&S and Labor Costs
- Specific deviations:
  - ⇨ Cost based on quotations: 30% contingency
    - sensors
    - power supplies
  - ⇨ A few high uncertainty items: 100% contingency
    - SVX4 chip layout cost estimates
    - L0 analogue cable production

	2002	2003	2004	2005	2006	Totals
% MS cont.	0.26	0.49	0.46	0.51		0.46
% Labor cont.	0.20	0.54	0.50	0.50		0.47

Schedule and Milestones

- The Base Schedule – No Contingency
  - ⇨ The schedule is constructed based on how long we think it will take to perform the tasks.
  - ⇨ has ~150 low level milestones scattered over the project
  - ⇨ End date is 4/21/05
  - ⇨ used to aggressively manage the project.
- Level 2 Milestones (includes contingency)
  - ⇨ Subset of low level milestones but dates include contingency
  - ⇨ 17 Level 2 milestones, ~1/quarter
  - ⇨ Reported to Directorate and DOE project manager
  - ⇨ End date with contingency is 12/22/05
  - ⇨ Use of the contingency will be managed within the project, Fermilab and DOE project manager via change orders (similar to money contingency)

Contingency and Milestones

Reportable Level 2 Milestones	Date	Cont.
1st Chip ready for hybrids	07/15/02	
Prototype Stave #1 available - Reporting	11/12/02	4 wks
Production Sensor submission (axials) - Reporting	12/20/02	4 wks
Testing of Prototype DAQ Chain Complete- go ahead for #2	03/18/03	8 wks
Production chip Submission - Reporting	07/17/03	8 wks
all tests of stave installation, screen mounting, complete	08/22/03	8 wks
Go ahead for DAQ Preproduction	09/05/03	8 wks
Bulkheads Complete	03/24/04	12 wks
Go ahead for DAQ Production	04/06/04	12 wks
L0 prototype modules complete	05/11/04	8 wks
Production Staves Available	10/08/04	20 wks
L0 Supports Complete	10/18/04	16 wks
Stave installation begins	01/13/05	20 wks
Stave installation complete	07/18/05	28 wks
Inner Detector Complete	07/01/05	24 wks
Outer Detector Complete	09/27/05	32 wks
SVX2b Ready for Installation into ISL	12/22/05	34 wks

Schedule Contingency and Milestones

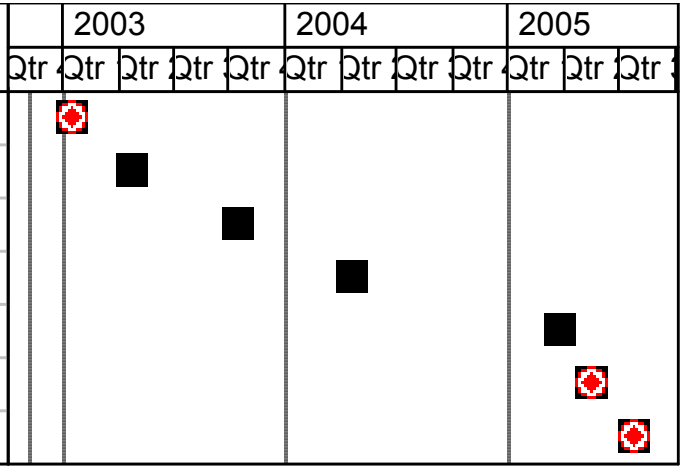
- Contingency on Level 2 milestones was set by silicon project managers based on the risk of those tasks
- Total contingency on L2 ends up at 34 weeks, ~ 25% of total project length.
- Level 1 Milestones (highest level)
  - ⇨ Subset of Level 2 milestones but includes an additional 47 weeks (~34%) of contingency
  - ⇨ We report on these to DOE headquarters

Reportable Level 1 Milestones	Date	Cont.
Production Staves Available	9/20/05	47 wks
Outer Detector Complete	8/31/06	47 wks
SVX2b Ready for Installation into ISL	11/23/06	47 wks

Schedule: Critical Path

Critical Path Level 3 Milestones
(*Level 3 = Level 2 without the contingency)

sk Name	Start
1.3.4.1.12 Prototype Stave #1 available	Tue 10/15/02
1.1.9.2.3 Testing of Prototype DAQ Chain Complete- go ahead fo	Tue 1/21/03
1.1.9.2.6 Go ahead for Preproduction	Thu 7/10/03
1.1.9.3.4 DAQ Production Go-Ahead	Tue 1/13/04
1.7.1.3.5 Stave installation complete	Tue 12/21/04
1.7.1.3.12 Outer Detector Complete	Thu 2/10/05
1.7.3.5.7 SVX2b Ready for Installation into ISL	Thu 4/21/05

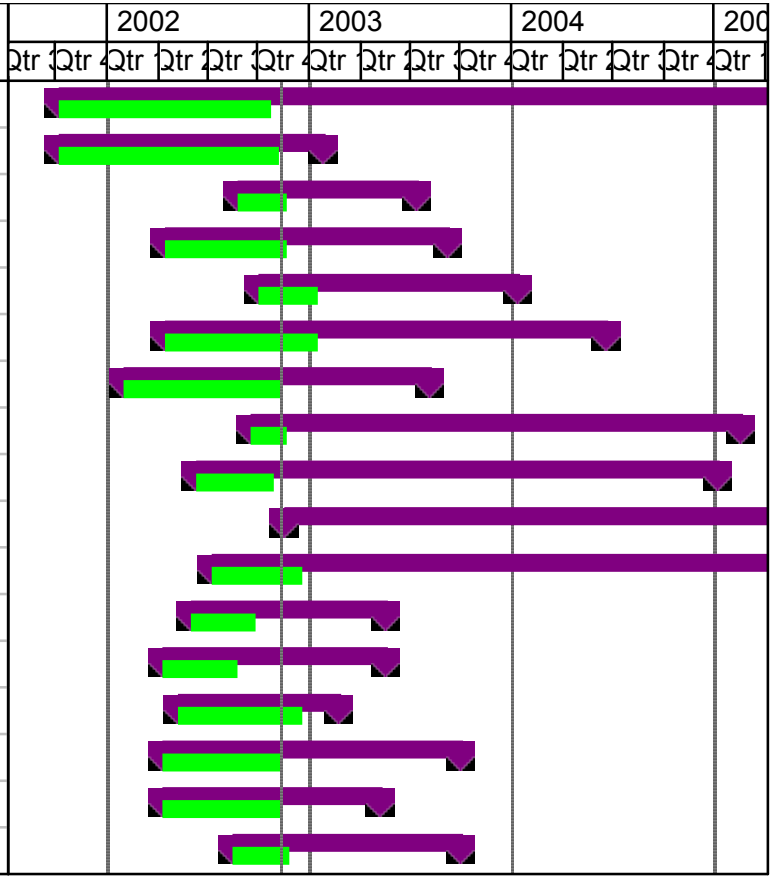


Schedule is driven by production and testing of outer layer stave components: Hybrids, Bus Cable, Mini-Portcard

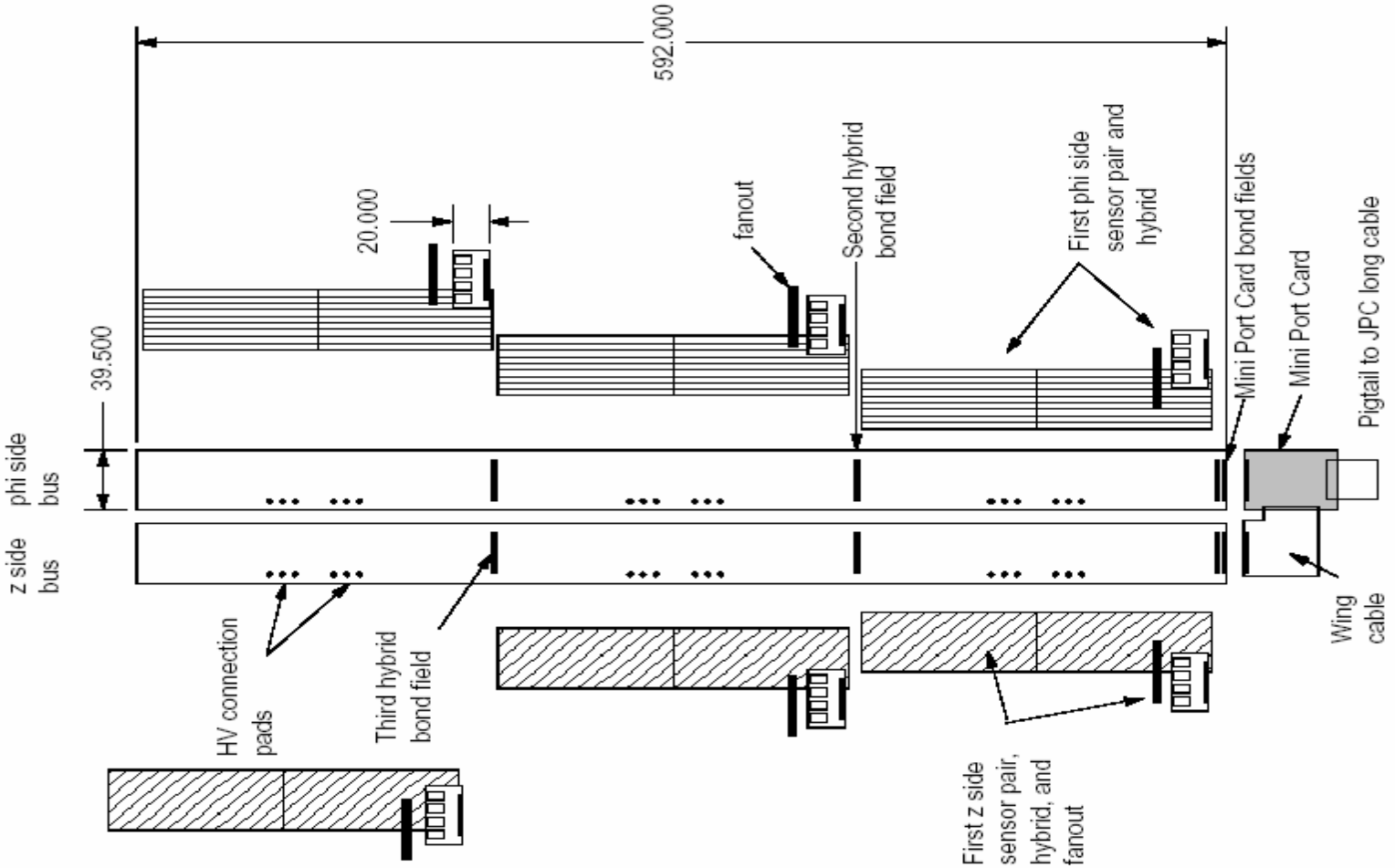
Status

- We have prototype parts and are just starting to build prototype modules and staves - On track for 1st prototype stave milestone 10/15/02

WBS	Name	Start
1.1.1	**DAQ Prototypes**	**Mon 7/2/01**
1.1.1.12	**SVX4 chip: 1st Prototype**	**Mon 7/2/01**
1.1.1.2	**Transceiver Chips**	**Wed 5/22/02**
1.1.1.13	**Outer Hybrid prototypes**	**Fri 1/11/02**
1.1.1.14	**Layer 0**	**Mon 7/1/02**
1.1.1.4	**Bus Cables**	**Fri 1/11/02**
1.1.1.15	**Mini Port Card Prototypes**	**Mon 10/29/01**
1.1.1.6	**Junction Port Cards**	**Mon 6/17/02**
1.1.1.7	**Cables**	**Fri 3/8/02**
1.1.1.9	**DAQ Testing & Readiness**	**Mon 8/12/02**
1.1.1.10	**Power Supply system**	**Fri 4/5/02**
1.1.14	**Outer Layers Module Prototype**	**Thu 2/28/02**
1.1.15	**Outer Layer Stave Prototype**	**Mon 1/7/02**
1.1.13	**Outer Sensors Prototype**	**Mon 2/4/02**
1.1.5	**Support Mechanics**	**Mon 1/7/02**
1.1.5.8	**Bulkhead Prototype work**	**Mon 1/7/02**
1.1.5.9	**Layer 0 CF support prototype**	**Mon 5/13/02**

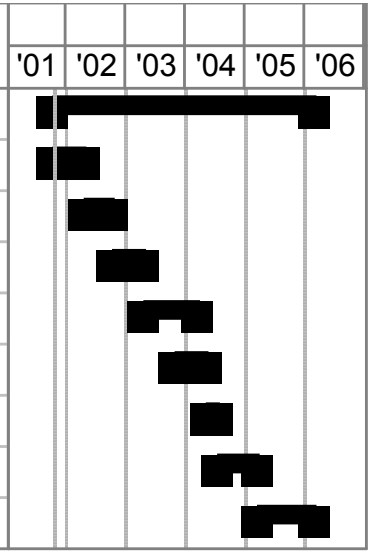


Stave Components



Critical Path Summary Schedule

Task Name	Duration	Start	Finish
Silicon Project	**1091 days**	**Mon 7/15/02**	**Thu 11/23/06**
Stave Prototype Round 1	**126 days**	**Mon 7/15/02**	**Tue 1/21/03**
Stave Prototype Round 2	**120 days**	**Wed 1/22/03**	**Thu 7/10/03**
Stave Preproduction Round	**120 days**	**Fri 7/11/03**	**Tue 1/13/04**
Stave Production	**235 days**	**Wed 1/14/04**	**Tue 12/14/04**
Installation	**135 days**	**Fri 7/23/04**	**Thu 2/10/05**
Final Assembly	**50 days**	**Fri 2/11/05**	**Thu 4/21/05**
Level 2 Contingency	**170 days**	**Fri 4/22/05**	**Thu 12/22/05**
Level 1 Contingency	**235 days**	**Fri 12/23/05**	**Thu 11/23/06**

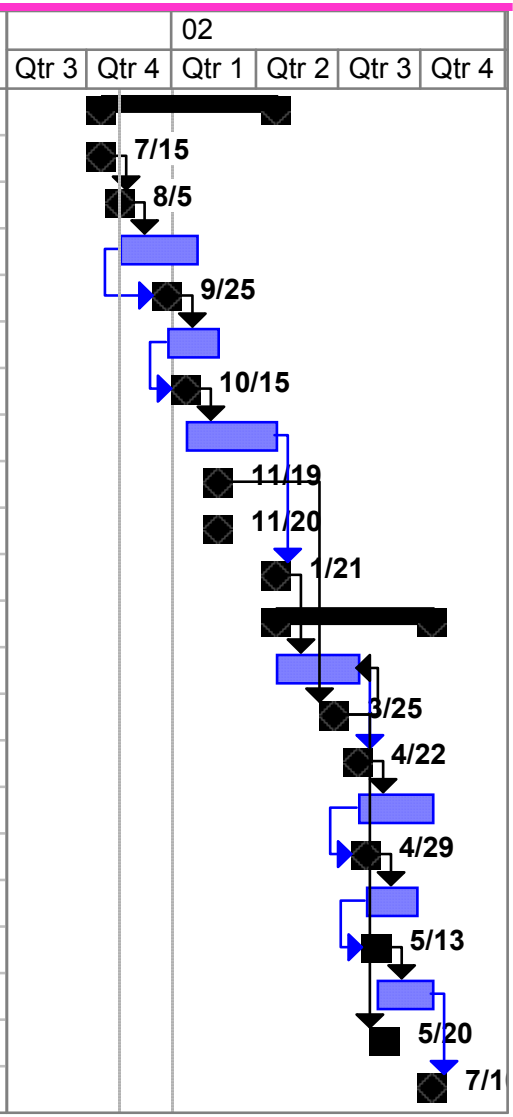


Each Round has all stave components: hybrids, bus cables, MPC

Total base project length 137 weeks (686 days)
Contingency on base schedule for L2 milestones = 34 weeks (25%)
Additional contingency for Level 1 = 47 weeks (total of 59%)

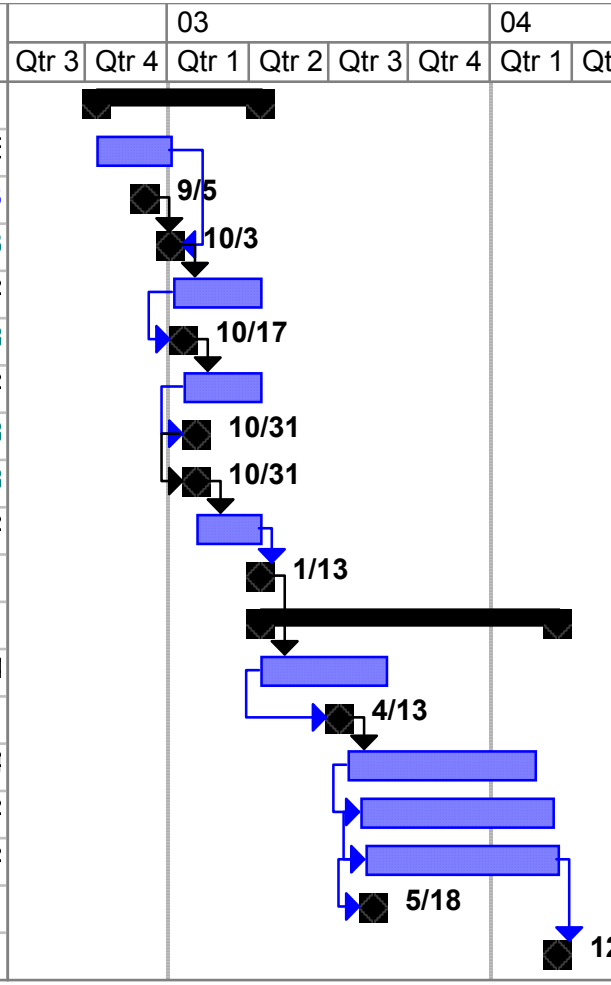
Critical Path Details: Stave Prototype Rounds 1 and 2

Task Name	Duration	Start	Finish
Stave Prototype Round 1	**126 days**	**Mon 7/15/02**	**Tue 1/21/03**
1st prototype SVX4 chips ready for hybrids	**0 days**	**Mon 7/15/02**	**Mon 7/15/02**
1st hybrids available	**0 days**	**Mon 8/5/02**	**Mon 8/5/02**
module assembly	60 days	Mon 8/5/02	Mon 10/28/02
Ready to begin electrical stave assembly	**0 days**	**Wed 9/25/02**	**Wed 9/25/02**
Prototype Stave: electrical assembly	40 days	Wed 9/25/02	Tue 11/19/02
Prototype Stave #1 available	**0 days**	**Tue 10/15/02**	**Tue 10/15/02**
Testing of Prototype DAQ Chain	60 days	Wed 10/16/02	Tue 1/21/03
preproduction SVX4 chip submission	**0 days**	**Tue 11/19/02**	**Tue 11/19/02**
production sensor submission	**0 days**	**Wed 11/20/02**	**Wed 11/20/02**
Go ahead for Stave #2 prototype round	**0 days**	**Tue 1/21/03**	**Tue 1/21/03**
Stave Prototype Round 2	**120 days**	**Wed 1/22/03**	**Thu 7/10/03**
Hybrid #2, MPC #2 manufacturing	65 days	Wed 1/22/03	Tue 4/22/03
preproduction SVX4 chips ready for hybrids	**0 days**	**Tue 3/25/03**	**Tue 3/25/03**
Hybrid, MPC #2 available	**0 days**	**Tue 4/22/03**	**Tue 4/22/03**
Prototype #2 module assembly	55 days	Wed 4/23/03	Thu 7/10/03
Prototype #2 modules available	**0 days**	**Tue 4/29/03**	**Tue 4/29/03**
Prototype #2 Stave: electrical assembly	40 days	Wed 4/30/03	Wed 6/25/03
Prototype #2 Stave available	**0 days**	**Tue 5/13/03**	**Tue 5/13/03**
Testing of proto #2 DAQ chain	40 days	Wed 5/14/03	Thu 7/10/03
Production SVX4 Chip Submission	**0 days**	**Tue 5/20/03**	**Tue 5/20/03**
Go ahead for Preproduction	**0 days**	**Thu 7/10/03**	**Thu 7/10/03**



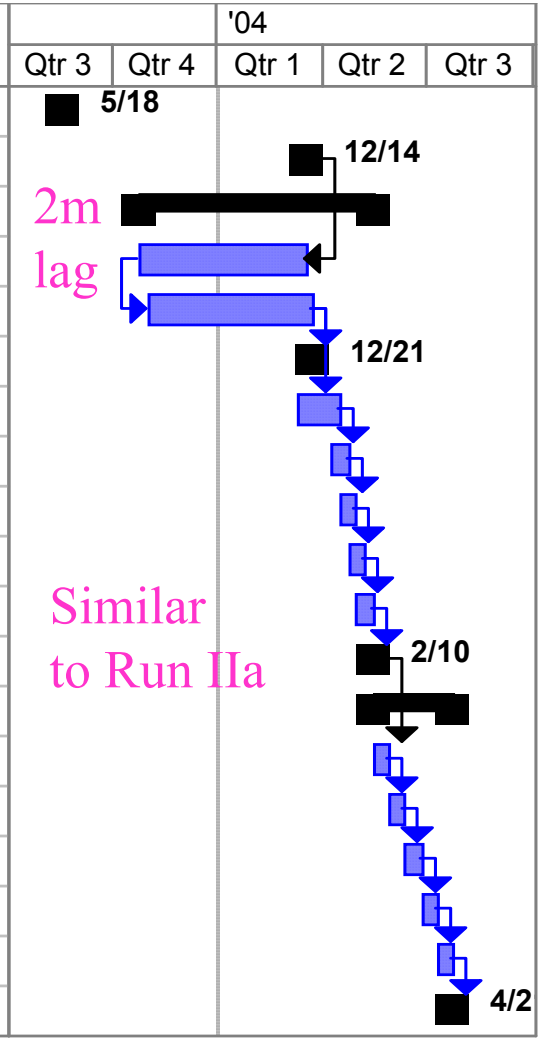
Critical Path Details: preproduction and production

sk Name	Duration	Start	Finish
Stave Preproduction Round	**120 days**	**Fri 7/11/03**	**Tue 1/13/04**
hybrid, MPC, Bus Cable manufacturing	60 days	Fri 7/11/03	Fri 10/3/03
Production SVX4 chips ready for hybrids	**0 days**	**Fri 9/5/03**	**Fri 9/5/03**
Preproduction Hybrid Available	**0 days**	**Fri 10/3/03**	**Fri 10/3/03**
Preproduction module: Assembling	60 days	Mon 10/6/03	Tue 1/13/04
Preproduction modules available	**0 days**	**Fri 10/17/03**	**Fri 10/17/03**
Preproduction Stave: electrical assembly	50 days	Mon 10/20/03	Tue 1/13/04
Preproduction Stave: electricals available	**0 days**	**Fri 10/31/03**	**Fri 10/31/03**
Ready to test PreProduction DAQ chain	**0 days**	**Fri 10/31/03**	**Fri 10/31/03**
Testing of Preproduction DAQ chain	40 days	Mon 11/3/03	Tue 1/13/04
Go ahead for Production	**0 days**	**Tue 1/13/04**	**Tue 1/13/04**
Stave Production	**235 days**	**Wed 1/14/04**	**Tue 12/14/04**
Hybrid, MPC, Bus cable manufacturing	100 days	Wed 1/14/04	Wed 6/2/04
Production hybrids available	**0 days**	**Tue 4/13/04**	**Tue 4/13/04**
Production Modules: Assembling	150 days	Wed 4/21/04	Fri 11/19/04
Production Stave: electrical assembly	150 days	Wed 5/5/04	Tue 12/7/04
Production Stave: electrical testing	150 days	Wed 5/12/04	Tue 12/14/04
Production Staves available	**0 days**	**Tue 5/18/04**	**Tue 5/18/04**
Stave Production Complete	**0 days**	**Tue 12/14/04**	**Tue 12/14/04**



Critical Path Details: Final assembly

Task Name	Duration	Start	Finish
Production Staves available	**0 days**	**Tue 5/18/04**	**Tue 5/18/04**
Stave Production Complete	**0 days**	**Tue 12/14/04**	**Tue 12/14/04**
Installation	**135 days**	**Fri 7/23/04**	**Thu 2/10/05**
Installation of staves	100 days	Fri 7/23/04	Tue 12/14/04
Installation of Stave: electrical test	100 days	Fri 7/30/04	Tue 12/21/04
Stave installation complete	**0 days**	**Tue 12/21/04**	**Tue 12/21/04**
Final system tests	20 days	Wed 12/8/04	Thu 1/13/05
installation of outer screen	10 days	Fri 1/7/05	Thu 1/20/05
remove axle	10 days	Fri 1/14/05	Thu 1/27/05
Installation of barrel in spacetube	10 days	Fri 1/21/05	Thu 2/3/05
dressing of cables and cooling	10 days	Fri 1/28/05	Thu 2/10/05
Outer Detector Complete	**0 days**	**Thu 2/10/05**	**Thu 2/10/05**
Final Assembly	**50 days**	**Fri 2/11/05**	**Thu 4/21/05**
Combine Inner and Outer Detecto	10 days	Fri 2/11/05	Thu 2/24/05
Install Beampipe and supports	10 days	Fri 2/25/05	Thu 3/10/05
Final survey	10 days	Fri 3/11/05	Thu 3/24/05
Final Cooling and electrical Tests	10 days	Fri 3/25/05	Thu 4/7/05
Close top of spacetube(final dress	10 days	Fri 4/8/05	Thu 4/21/05
SVX2b Ready for Installation int	**0 days**	**Thu 4/21/05**	**Thu 4/21/05**



Final Assembly: Comparison to IIa

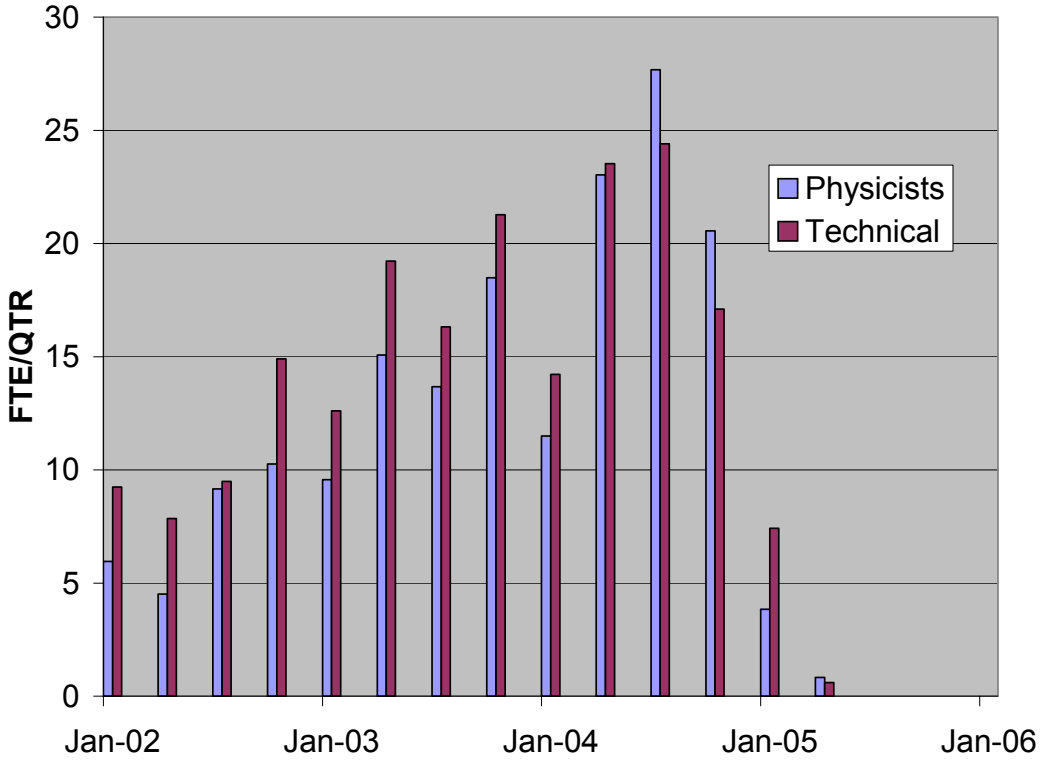
- Many Run IIb installation and final assembly tasks are similar to Run IIa
- Installation
  - ⇨ Run IIa average rate was 12 ladders installed and tested/week (peak was 18 ladders in one week)
  - ⇨ Run IIb schedule allows for 10 staves/week (2/day)
  - ⇨ Installation was (and will be) paced by ladder (stave) availability and testing time.
- Memorable dates in Run IIa final assembly
  - ⇨ Nov. 27th L00 (and beam-pipe) installed in SVX
  - ⇨ Dec. 17th Ready to install in ISL (~3 weeks)
  - ⇨ Run IIb schedule has 5 weeks

Labor

- Schedule includes time to perform each task
- To convert to FTE we apply an efficiency factor of 0.7
  - ⇨ 1456 hours of productive work per person per year (364 hr/qtr)

Labor totals for Technical personnel and Physicists in base schedule

Note that contingency Labor is not included in the plot

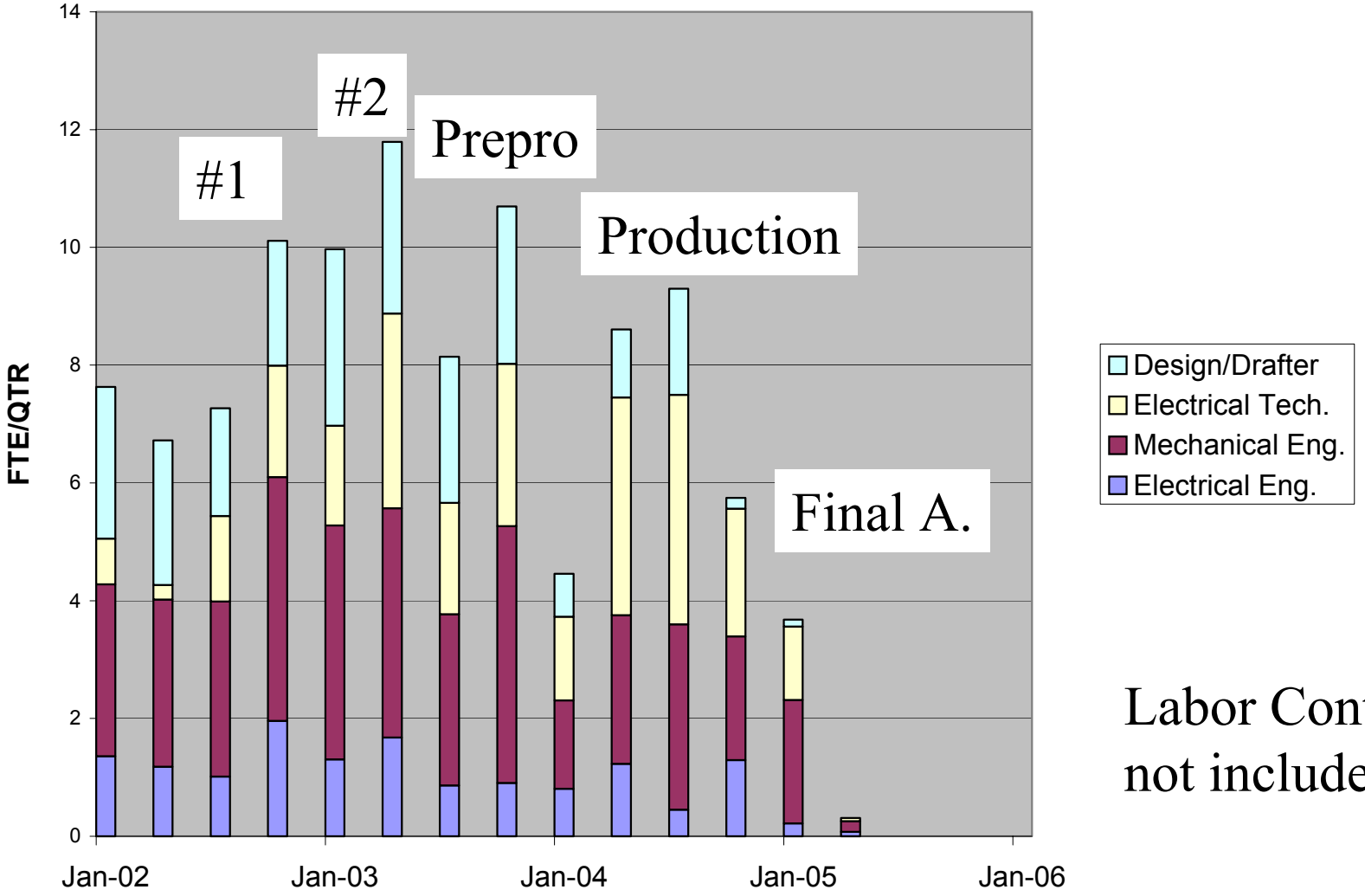


Run IIb Silicon Institutions

CMU
JH
LBL
Wayne St.
Toronto
Rome
Tsukuba
Davis
Fermilab
Helsinki
U of I
Duke
UCSB
Padova
Bologna
Okayama
Rutgers
Korea
Academia Sinica
Purdue

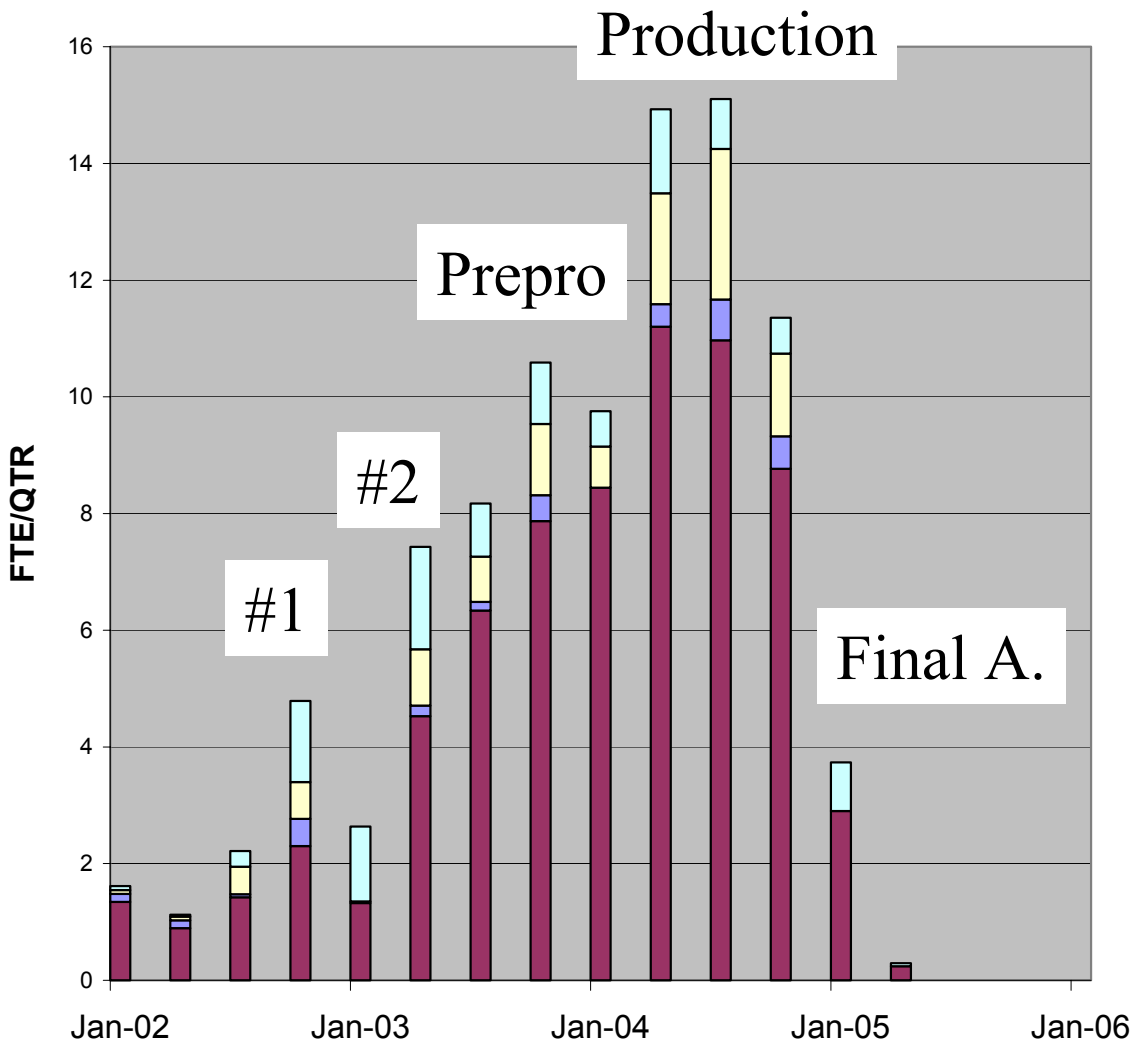
- 20 institutions have expressed interest thus far
- Negotiations with additional institutions are in progress

Engineering and associated support



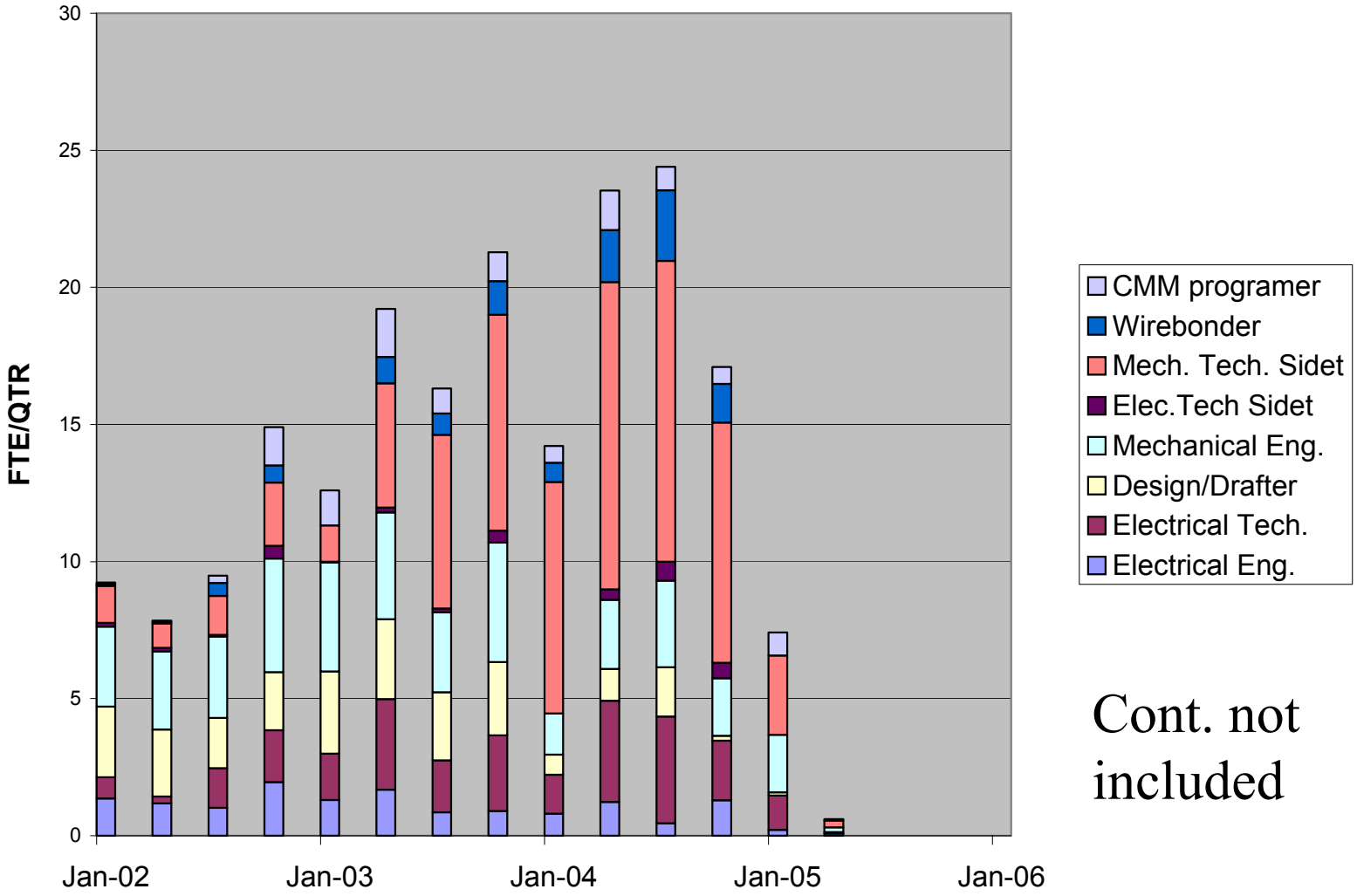
Labor Cont. not included

Sidet Technical Staff



Cont. not included

Technical Labor Total



Cont. not included

Risk Assessment: Silicon Project

Evaluating Impact of a Risk on Major Project Objectives					
Project Objective	**Very low 0.05**	**Low 0.1**	**Moderate 0.2**	**High 0.4**	**Very high 0.8**
Cost		$100K - $200K increase	$200K-$500K increase	$500K - $1M increase	> $1M increase
Schedule		slippage 1 - 2 months	slippage 2-4 months	slippage 4-8 months	slippage > 8 months
Technical			technical performance affected but still acceptable	degradation of technical performance unacceptable for physics objectives	

Based on Risk assessment table in the project management plan (Ref. Text: A guide to the Project Management Body of Knowledge PMBOK Guide 2000 Ed.)

- ⇨Scope impact factors not estimated: assume scope reductions would only be imposed as mitigation for catastrophic overruns of cost or schedule
- ⇨Two categories for technical impact

Risk Assessment

- Risk analysis performed by Project manager for CDF Run IIa Silicon project (Jeff Spalding)
  - ⇨ ~ independent review of cost and schedule risk
- Risk assessment document lists risks associated with Level 4 summary tasks, with more detailed analysis for critical tasks

Mitigation of Risks in Base Schedule

- Cost risk mitigated by attaching contingency to each task
  - Total cost contingency ~50% (M&S + Labor)
- Schedule risk mitigated by including contingency lag time on major milestones. This contingency time will be managed with change orders similar to cost contingency.
  - Total Schedule contingency = 34 weeks at Level 2 (~25%)
- Technical Risk mitigated by:
  - extensive testing time
  - 2 prototype rounds for all stave components
  - preproduction submission
  - production submission

Risk Assessment: Schedule Conclusions

Milestone	Est Sched Impact (wks)	Est Sched Risk	Cumulative contingency needed (wks)	Milestone Lag (wks)
Production chip Submission - Reporting	8-16	0.4	12	8
Go ahead for DAQ Production	8-16 8-16 4-8	0.1 0.4 0.2	24	12
Production Staves Available	4-8	0.2	30	20
Stave installation complete	4-8	0.4	34	28
Outer Detector Complete	4-8 4-8	0.2 0.2	38	32
SVX2b Ready for Installation into ISL			**38**	**34**

Different choice for distribution of contingency within the project

Contingency is distributed based on L2 PM risk assessment

External Risk A. suggests putting more contingency earlier in project.

Total contingency estimates are in good agreement

Risk Assessment Conclusions: Cost and Technical

- Cost risk adequately covered by allocated contingency
- Technical risk: moderate
  - ⇨ Main areas of concern
    - chip noise performance
    - DAQ bandwidth
    - mechanical alignment of final detector
  - ⇨ Risk mitigated by extensive prototyping and testing
  - ⇨ Unlikely that performance degradation would be severe enough to seriously impact physics capabilities

Conclusions

- We have presented our resource loaded schedule
- Critical path is dominated by production and testing of outer layer staves

Total Silicon Project Costs

Costs are in Then year $ and include overhead

	2002	2003	2004	2005	2006	Totals
M&S	843,793	3,616,256	4,365,894	330,078	-	9,156,022
M&S Cont.	218,914	1,778,400	2,012,040	169,843	-	4,179,197
Labor	502,549	1,055,130	1,292,582	419,191	-	3,269,451
Labor Cont.	102,581	571,938	649,754	209,511	-	1,533,784
Total	**1,667,837**	**7,021,723**	**8,320,270**	**1,128,623**	**-**	**18,138,454**

Risk Assessment analysis found:
Cost Risk adequately covered by contingency
Technical Risk covered by multiple prototype rounds
Schedule Risk covered by contingency on Level 1 and 2 milestones